Amendments to the Specification:

Please replace the paragraph beginning on page 19, line 21 with the following rewritten paragraph:

According to the present invention, a coefficient ramping circuit is utilized to gradually provide tap coefficients from the feedback filter of a receiver, such as that of a DSL transceiver, to a precoder, typically a Tomlinson-Harashima precoder, of a transmitter, such as that of a DSL transceiver. The coefficient ramping circuit is configured to provide a ramped output for at least one of the decision feedback filter tap coefficients. The coefficient ramping circuit is typically configured to provide a ramped output for all of the decision feedback filter tap coefficients. The ramped output is ramped over time from a first value to a second ~~to a second~~ value. The second value typically depends upon the converged value of the feedback filter tap coefficient(s).

B1

Please replace the paragraph beginning on page 28, line 11 with the following rewritten paragraph:

Referring now to FIG. 3, according to the present invention, a decision feedback equalizer 30 includes a feedforward filter 20 having a reference tap 23d (FIG. 2) located proximate a center thereof. The feedforward filter 20 provides an output to adder 33. An output of the adder 33 is provided to slicer 35. The slicer 35 provides an error signal output to the feedforward filter 20 and also to a decision feedback filter 37. The feedforward filter 20 and the decision

B2 cont

B2 Cont'd

feedback filter 37 use the error signal to vary the coefficients of the taps of the feedforward filter 20 and the decision feedback filter 37, according to well-known principles. The decision feedback filter 37 provides an output to adder 33.

Please replace the paragraph beginning on page 29, line 28 with the following rewritten paragraph:

B3

FIG. 5 is a simplified block diagram of a system 50 in which two transceivers communicating over a channel, wherein ramped coefficients are transmitted over the channel according to the present invention. ~~With particular reference to~~As shown in FIG. 5, ~~according to the present invention,~~ tap coefficients from a decision feedback filter 57 of receiving transceiver 53 are ramped and communicated to a Tomlinson-Harashima precoder 503 of transmitting transceiver 501.

Please replace the paragraph beginning on page 32, line 10 with the following rewritten paragraph:

B4 Cont

FIG. 6 is a simplified block diagram of a system 60, in which two transceivers communicating over a channel, wherein unramped coefficients are transmitted over the channel according to the present invention. As shown in FIG. 6, adder 602 receives information to be transmitted and also receives an output of the Tomlinson-Harashima precoder 603. The adder 602 provides an output to transmitter 61 and to Tomlinson-Harashima precoder 603. Tomlinson-Harashima precoder 603 receives ramped coefficients from coefficient ramping circuit 604. Coefficient ramping circuit 604 receives unramped coefficients from decision

B4 cont'd

feedback filter 67 of the receiving transceiver 63 via channel 62.

Please replace the paragraph beginning on page 33, line 28 with the following rewritten paragraph:

subc7

With particular reference to FIG. 7, cooperation of the coefficient ramping circuit 604 with the Tomlinson-Harashima precoder 603, both also of FIG. 6, is shown. Cooperation of the coefficient ramping circuit 504 with the Tomlinson-Harashima precoder 503, both of FIG. 5, is similar, with the outputs 79a-79b of the coefficient ramping circuit 604 being communicated via the channel 62, rather than being communicated solely within the transmitting transceiver 601. As those skilled in the art will appreciate, Tomlinson-Harashima precoder 603 includes a plurality of delay registers 71a-71d, the output of each of which is modified by taps 73a-73d. Taps 73a-73d contain coefficients p_1-p_N, respectively. The outputs of taps 73a-73d are summed by adders 75a-75c and the outputs of adders 75a-75c are combined with the information to be transmitted via adder 602. Mod2 77 truncates or rounds the output of adder 602 to provide the desired number of bits b_n for input to transmitter 61 (FIG. 6).

B5

Please replace the paragraph beginning on page 35, line 23 with the following rewritten paragraph:

Referring now to FIG. 8, an exemplary implementation of both aspects of the present invention in a digital subscriber line-up (DSL) system 80 is shown. More particularly, a DSL

B6 cont'd

B6 Cont'd

modem 82 contains a first transceiver and a digital switch 87 contains a second transceiver. The DSL modem 82 facilitates communication of a plurality of telephones 83, 84 and 86, as well as personal computer (PC) 85 with both the public switched telephone (PSTN) network 88 and a packet network 89.

Please replace the paragraph beginning on page 36, line 16 with the following rewritten paragraph:

B7

Incoming information from the hybrid circuit is provided to analog filter 98, autogain circuit 99 and digital-to-analog converter ~~91~~ 901. Echo canceller 902 operates upon the analog output of digital analog converter 901 to mitigate the undesirable effects of echos.

Please replace the paragraph beginning on page 36, line 21 with the following rewritten paragraph:

B8

Adaptive equalizer 903 includes the decision feedback equalizer 57, 67 of the present invention, which includes the feedforward filter 20 and decision feedback filter 37 of FIG. 3 and/or the feedforward filter 54, 64 and decision feedback filter 57, 67 of FIGs. 5 and 6. The symbols are then recovered from the output of the adaptive equalizer 903 by symbol recovery 904 and errors are decoded by error decoding 905.